



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Fernando Gonzalez, et al.

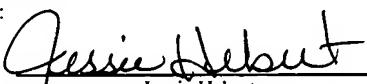
Serial No.: 10/751,141

Filed: December 31, 2003

For: Transistor Having Vertical
Junction Edge and Method of
Manufacturing the Same

§ Group Art Unit: 2815
§
§ Examiner: Nguyen, Joseph H.
§
§ Atty Docket: MICS:0114/MAN
§ 02-1010

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: OFFICIAL DRAFTSMAN

CERTIFICATE OF MAILING 37 C.F.R. 1.8	
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:	
April 19, 2007	 Jessie Hebert
Date	Jessie Hebert

Sir:

TRANSMITTAL OF FORMAL DRAWINGS

Enclosed are Replacement Sheets for three of the five originally submitted sheets, wherein minor informalities have been formalized. Applicants respectfully submit that no new matter has been added.

Respectfully submitted,



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Date: April 19, 2007